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| EXAMINER | |
|---|---|
| KIM, DAVID S | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/764,605 | HARTZELL ET AL. | |
| | Examiner | Art Unit | |
| | David S. Kim | 2613 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Applicant's response to the objection to claim 4 in the previous Office Action (mailed on 02 February 2007) is noted and appreciated. Applicant responded by amending claim 4. Applicant's amendment overcomes the previous objection, which is presently withdrawn.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 3-9, and 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky et al. (U.S. Patent No. 4,766,471, hereinafter "Ovshinsky") in view of Ramaswami et al. (*Optical Networks: A Practical Perspective, 2nd ed.*, hereinafter "Ramaswami"), Peters et al. (U.S. Patent No. 5,323,520, hereinafter "Peters") and Bartur et al. (U.S. Patent Application Publication No. US 2003/0142929 A1, hereinafter "Bartur").

**Regarding claim 1**, Ovshinsky discloses:

A transceiver system, comprising:

a transmitter portion (e.g., 1st layer in Fig. 16A with transmitter elements of col. 30, l. 10-13) arranged on a bottom layer (1st layer in Fig. 16A would be on the "bottom" if viewed upside-down) of a multi-layer board (e.g., 540), the transmitter portion capable of providing signals to a transmitter optical subassembly;

a receiver portion (e.g., 1st layer in Fig. 16A with receiver elements of col. 30, l. 40-48) arranged on the bottom 1st layer in Fig. 16A with transmitter elements of col. 30, l. 10-13) layer of the multi-layer board (e.g., 540), the receiver portion capable of receiving signals from a receiver optical subassembly.

Ovshinsky does not expressly disclose:

a ***high-voltage power supply*** arranged on a ***top*** layer of the multi-layer board, the high-voltage power supply providing a ***bias voltage*** for the receiver optical sub assembly; and

a ***metallic ground plane*** arranged on a first intermediate layer between the top layer and the bottom layer, the metallic ground plane providing ***electrical isolation*** between the high-voltage power supply and the transmitter portion and the receiver portion.

Regarding the limitation of a ***power supply***, notice that one would obvious implement some kind of power supply for the various components of the apparatus of Ovshinsky.

Regarding the limitation of a ***high-voltage*** power supply, notice that Ovshinsky broadly discloses the use of various type of receiver elements (col. 30, l. 40-48). Another well-known type of receiver element is disclosed by Ramaswami, such as an avalanche photodiode (p. 197, APDs). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to employ other alternate types of receiver elements, such as an APD. One of ordinary skill in the art would have been motivated to do this for other benefits that they may have over other types of receiver elements. For example, an APD has greater responsitivity than other types of receiver elements (Ramaswami, p. 197, 1st full paragraph). An APD generally requires a ***high-voltage power supply for bias voltage***, so an obvious variation of Ovshinsky with an APD would also employ a ***high-voltage power supply for bias voltage***.

Regarding the limitations of arranging a power supply on a ***top*** layer of a multi-layer board, the ***metallic ground plane***, and the ***electrical isolation***, notice that the practice of locating a power supply and other circuitry on opposite sides of a multi-layer board is known in the art, as shown by Peters (Fig. 1, power supplied from layer 2 to circuitry on layer 1). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to locate the power supply and the transmitter and receiver portions on opposite sides of the multi-layer board (power supply on the ***top*** layer), as exemplified by Peters. One of ordinary skill in the art would have been motivated to do this since doing so would result in isolating the power supply layer from other layers, which would reduce the undesired possibility of shorting (Bartur, end of paragraph [0051]). That is, among all of the various locations to

place an isolated power supply layer, the opposite side of the multi-layer board from the transmitter and receiver portions is a suitable location. In such a position, the ***metallic ground plane*** of Peters (Peters, plate 6 connected to ground 7 in Fig. 2) would be located between the power supply and the transmitter and receiver portions, providing ***electrical isolation*** therebetween.

**Regarding claims 3-5**, Ovshinsky in view of the references applied above (hereinafter the "RAA") does not expressly disclose:

(claim 3) The system according to claim 1, wherein a second intermediate layer having vias is arranged between the first intermediate layer and the top layer.

(claim 4) The system according to claim 1, wherein a third intermediate layer having vias is arranged between the first intermediate layer and the bottom layer.

(claim 5) The system according to claim 4, wherein an interconnect layer is arranged between the first intermediate layer and the third intermediate layer.

However, Ovshinsky does disclose the use of multiple layers (Ovshinsky, Fig. 16A), and the use of vias is well known for connecting multiple layers (Peters, vias for 7 and 8 in Fig. 2; Bartur, end of paragraph [0051]). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include any of these various layers and vias to provide obvious variants of the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this for any variety of suitable reasons, such as further insulation (Bartur, end of paragraph [0051]), reduction of the possibility of shorting (Bartur, end of paragraph [0051]), or addition of components and circuitry.

**Regarding claim 6**, Ovshinsky in view of the RAA does not expressly disclose:

The system according to claim 1, further including a microcontroller system arranged on the top layer and the bottom layer.

However, the use of a microcontroller system for a system, such the system of Ovshinsky in view of the RAA, is an extremely well known practice in the art. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to place a microcontroller system on the top and bottom layers. One of ordinary skill in the art would have been motivated to do this to locate

microcontroller components in close proximity of the circuits that they would control, such as the power supply of the top layer and the transmitter and receiver portions of the bottom layer.

**Regarding claims 7-9**, claims 7, 8, and 9 are claims that introduce limitations that correspond to the limitations all introduced by claim 1. Therefore, the recited limitations in claim 1 read on the corresponding limitations in claims 7-9.

**Regarding claim 11**, Ovshinsky in view of the RAA discloses:

The method of claim 8, further including arranging a first intermediate layer between the top layer and the bottom layer, the first intermediate layer including vias to provide electrical contact with traces on the top layer (e.g., Peters, via 16 or 17 in Fig. 11).

**Regarding claims 12-13**, Ovshinsky in view of the RAA does not expressly disclose:

(claim 12) The method of claim 11, further including arranging a second intermediate layer between the first intermediate layer and the intermediate layer, the second intermediate layer providing traces.

(claim 13) The method of claim 12, further including arranging a third intermediate layer between the intermediate layer and the bottom layer, the third intermediate layer including vias.

However, Ovshinsky does disclose the use of multiple layers (Ovshinsky, Fig. 16A). The use of vias is well known for connecting multiple layers (Peters, vias for 7 and 8 in Fig. 2; Bartur, end of paragraph [0051]). Also, the use of traces is also well known for connecting circuitry (Bartur, trace layer 290 in Fig. 2c). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include any of these various layers, vias, and traces to provide obvious variants of the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this for any variety of suitable reasons, such as further insulation (Bartur, end of paragraph [0051]), reduction of the possibility of shorting (Bartur, end of paragraph [0051]), or addition of components and circuitry.

**Regarding claim 14**, claim 14 is an apparatus claim that introduces limitations that correspond to the limitations introduced by system claim 1. Therefore, the recited means in apparatus claim 14 read on the corresponding means in system claim 1.

4. **Claims 2 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky in view of the RAA as applied to the claims above, and further in view of Nelson et al. (U.S. Patent No. 5,097,393, hereinafter "Nelson").

**Regarding claim 2**, Ovshinsky in view of the RAA does not expressly disclose:

The system according to claim 1, wherein the transmitter portion and the receiver portion are arranged in a split-ground arrangement.

However, split-ground arrangements are known in the art, as shown by Nelson (col. 12, l. 26-52). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to include such an arrangement in the system of Ovshinsky in view of the RAA. One of ordinary skill in the art would have been motivated to do this to provide electrical isolation (Nelson, col. 12, l. 27-28), which generally reduces electrical interference between various components. For example, one could provide electrical isolation between the transmitter portion and the receiver portion to reduce electrical interference between these portions.

**Regarding claim 10**, claim 10 is a method claim that introduces limitations that correspond to the limitations introduced by system claim 1. Therefore, the recited steps in method claim 10 read on the corresponding means in system claim 1.

## ***Response to Arguments***

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. In particular, notice the new application of the teachings from Ovshinsky in view of the RAA to address the present claims.

## ***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSK

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER